

# HPFC-6600/6640 Tachyon QE4

## Quad-Channel 4 Gb Enhanced Fibre Channel PCI-Express Controller With T10 DIF

Preliminary  
Product Brief

### PRODUCT OVERVIEW

The Tachyon QE4 device (HPFC-66xx Series) is a high-performance 4-port 4 Gbit/s Fibre Channel controller. It features an 8-lane, native PCI Express bus, enabling full-duplex operation. QE4 is an integrated single chip solution ideal for a variety of high-performance I/O applications.

The Tachyon proven State-Machine architecture scales directly with system CPU performance and is not limited by the constraints of an embedded microprocessor. QE4 supports up to 4 processors per FC link using 4 independent register and API (Application Programming Interface) queue structures. This feature allows systems to scale to required performance as necessary while maintaining compatibility with the Tachyon programming model at the register level, and with the Tachyon Software Development Kit (TSDK) API tools.

The QE4 supports the T10 Standard Protection Information Model as described in the SCSI Block Commands - 2 (SBC-2) Standard, which incorporates a Data Integrity Field (DIF) in data records. Additionally, the QE4 has masking capabilities for enhanced functionality. T10 DIF provides a robust CRC-based data protection scheme with mechanisms to initiate, extend or terminate a protection domain, which can span both the PCI-Express interface and the Fibre Channel interface. When combined with Fibre Channel's standard CRC, T10 DIF offers complete data protection in the I/O data path. T10 DIF is performed in hardware to maximize performance.

QE4 offers additional performance by providing advanced frame-handling functions that are normally handled by the host processor. These additional enhancements make it possible for the system to utilize intelligent frame handling while reducing CPU utilization.

### APPLICATIONS

- Enterprise Storage Systems
- Embedded Subsystems
- Disk Arrays
- Multi-protocol Bridges/Routers
- Intelligent Switches
- Virtualization Devices



### FEATURES

- 4-port 4/2/1 Gb/s Fibre Channel controller
- TWI (Two-Wire Interface) control and presence detect for optical transceivers
- Multi DMA for cache mirroring
- CRC offload engine for enabling non-T10 DIF compliant solutions
- Enhanced TRE (Target Read Entry) for higher performance on small transfers (IOPS)
- ERQ (Exchange Request Queue)/SCSI LL (Linked List) priority control for additional Quality of Service control
- Support for up to 4 processors per FC Link
- Fibre Channel auto-speed negotiation
- PCI Express 8-lane 2.5 GHz Host Interface
- Supports 10Km distance per link at 4G link rate with internal memory
- Full duplex operation for each port
- T10 DIF protection
- Virtualization support with H/W assisted FC Frame Steering
- Pin compatible with Tachyon predecessor QX4 64xx series
- SCSI BiDi command assist
- Industry-leading technical support and documentation
- Software development API tools for Linux, and Windows
- Standard and RoHS compliant packages

## TACHYON ARCHITECTURE

The Tachyon architecture of the QE4 enables a complete hardware-based design in a single-chip FC solution. Numerous independent functional blocks concurrently process inbound data, outbound data, control and commands in hardware. This results in the lowest latency and the highest level of performance available today.

### DATA INTEGRITY FEATURES

- Variable block size support: 512/520 bytes
- SEST-based DIF
- CRC Offload Engine (COE)
- DIF per L/A (DPL)

### TACHYON EXPRESSWAY ARCHITECTURE

- Provides an interface from the Fibre Channel core to PCI Express
- Allows concurrent operation on each of the four 4 Gbit ports
- AER (Advanced Error Reporting) and Error ECN support
- MSI-X
- 4K PCI Express TLP

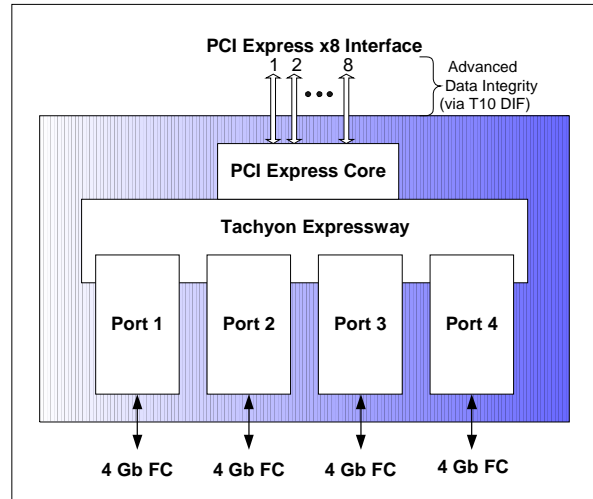
### PRELIMINARY SPECIFICATIONS

- Package Type: FC PBGA, 1mm ball pitch
- Power Dissipation: 5 Watts
- Thermal Specification: 0 - 110°C, T<sub>Junction</sub>
- Voltage Margin: ± 5%

### MAINTAIN TACHYON FIBRE CHANNEL FAMILY PROGRAMMING MODEL (SIMILAR TO THE QX4)

- Registers memory mapped
- Backward compatible offsets for Fibre Channel core registers

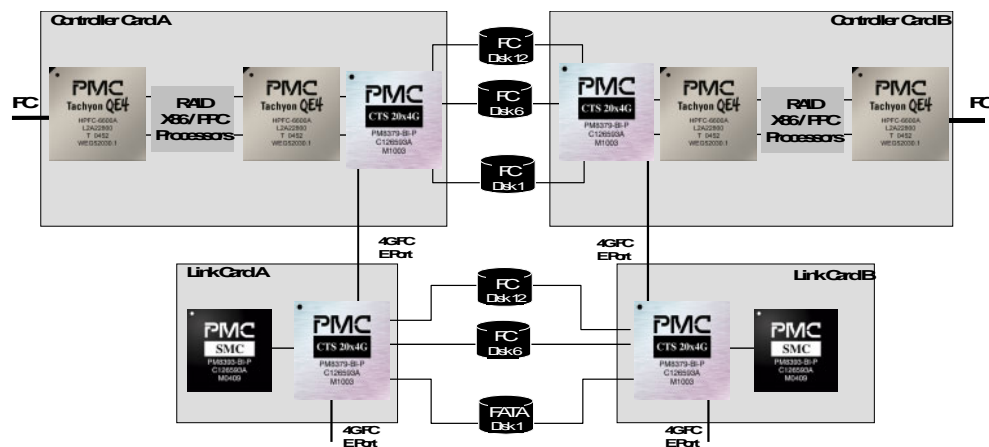
## QE4 HIGH-LEVEL BLOCK DIAGRAM



### STANDARD TACHYON FIBRE CHANNEL CORE FEATURE SET

- Performance scalable State Machine-based architecture
- Independent, concurrent inbound/outbound transaction processing
- Multiple outbound context support
- Support for SCSI initiator, target and initiator/target modes
- Complete sequence segmentation and reassembly done in hardware
- Up to 2048-byte frame payloads
- Fully assisted FC-FS Class 2 and Class 3 support
- ACK0/ACK1 models in hardware
- Interrupt avoidance mechanisms
- 64-bit addressing (44/45 bits per Length/Address pair)

## 4G SAN-ATTACHED FIBRE CHANNEL STORAGE SYSTEM APPLICATION



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